SYLLABUS FOR CUSTOM LAYOUT DESIGN

**Essentials of UNIX/Linux**

* Linux/UNIX OS, Shell
* Working with files, directories
* Commonly used commands

# *Semiconductor Basics*

* Conductor, Semiconductor & Insulators =( Intrinsic& Extrinsic) Semiconductor.
* Basic Passive and Active devices.
* Ohms law, Kirchoff laws
* Basic of circuit understanding

# *CMOS & FINFET Basics*

* MOSFET Basics, Operations, few simple circuits & second order effects.
* MOSFET Detailed fabrication process.
* FinFET working, Fabrication, advantages & disadvantages.

# *Layout tool*

* Layout Editor Tool
* Understanding the schematic symbols and parameters
* Creating and managing libraries and cell
* Commands for Layout editing.
* Commands for schematic editing.
* Verification : DRC and LVS
* Antenna effect, latchup, Electromigration, IR Drop
* Analog Layout of OpAmp, Current Mirror, PLL, ADC, and DAC
* Resistor, Capacitor layout techniques
* CMOS and BiCMOS layout techniques
* Standard Cell Layout : Inverter, AND, OR, NAND, NOR, AOI, OAI, Latches, and Flop

# *Advanced Layout Concepts*

* Mismatches & Matching.
* Failure Mechanism : Electro migration, IR drop, LOD & Stress effects, WPE, Antenna Effects, Latch up, ESD (with High voltage rules, EOS effects).
* Noises & Coupling.
* Different Types of process – Advantages & Disadvantages – Planar CMOS, FD-SOI, SOI, Bi- CMOS, Gallium Arsenide, Silicon-Germanium, Finfet.
* Full Chip Construction, Scribe Seal, Pad Frame, Integration and guidelines.
* Packaging.

# *Standard cell, IO, and Memory Layout*

* Std Cell & Memories.
* IO Layout Guidelines : High speed IOs and High Speed Interfaces.
* Sense amplifier & Bit cell development
* Why memory layout different than analog layout
* Memory layout flow
* Types of memory layout (SRAM/DRAM/ROM)
* Introduction to SRAM memory layout
* Fixing few manually created leaf-cell errors which impact
* Impact of IR, EM and DFM
* SRAM memory design architecture
* Words line and address line
* SRAM rows and column design
* Building blocks of SRAM
* Memory Bit cell
* Row decoder
* Word line driver
* Sense amplifier
* Control block
* Misc digital logic.
* Pitch Calculation for blocks.
* Power Planning

# *Analog and Mixed signal Layout*

* High speed Analog Layout
* RF Layout guidelines with Transmission lines and inductor concepts
* Handling clocks
* Analog Circuits & Layout guidelines
* Single &Multi stage differential opamp layout
* current mirror layout
* PLL, DLL and Oscillators
* LDO and other regulators
* ADCs & DACs
* Bandgap, Temperature sensors & Biases -> Current & Voltage bias lines
* input pair, differential routing, Power routing, offset minimizing
* Power/Signal IR Drop
* cross-talk and coupling
* Electrostatic Discharge
* Deep Submicron Layout Issues
* Shallow Trench Isolation (LOD)
* Well Proximity Effect.

# *Assignments and hands on projects*

* Assignments and multiple hands on projects
* Best Practices & Interview Questions.